HARRIS SEMICONDUCTOR

HM-92560

256K Synchronous CMOS RAM Module

January 1992

Features

- Low Standby Current..... 500µA
- Fast Address Access Time.....170ns
- Data Retention ..... 2.0V Min VCC
- Three-State Outputs
- Organizable as 32K x 8 or 16K x 16 Array
- On Chip Address Registers
- 48 Pin DIP Pinout .....2.66" x 1.30" x 0.29"
- Synchronous Operation .....30mA/MHz Yields Low Operating Power
- Operating Temperature Range .....-55°C to +125°C

Ordering Information

PACKAGE	TEMP. RANGE	150ns
Module	-55°C to +125°C	HM5-92560-8

Description

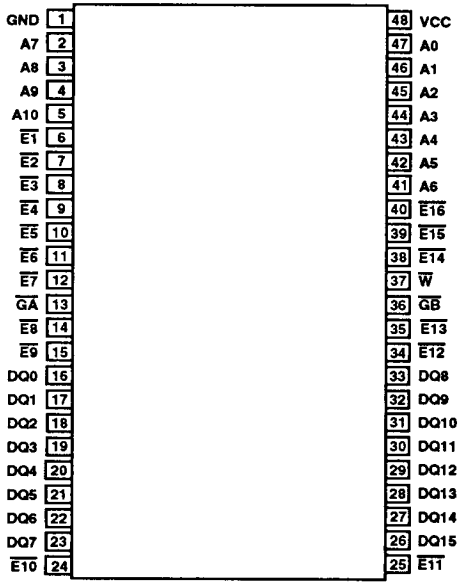
The HM-92560 is a high density 256K bit CMOS RAM module. Sixteen synchronous HM-6516 2K x 8 CMOS RAMs in Leadless Chip Carriers are mounted on a multilayer ceramic substrate. The HM-92560 RAM module is organized as two 16K x 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses and chip enables allow the user to format the HM-92560 as either a 16K x 16 or 32K x 8 array. Ceramic capacitors are included on the substrate to reduce noise and to minimize the need for additional external decoupling.

The synchronous design of the HM-92560 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

The HM-92560 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This package technique combines the high packing density of CMOS and Leadless Chip Carriers with the ease of use of DIP packaging.

Pinout

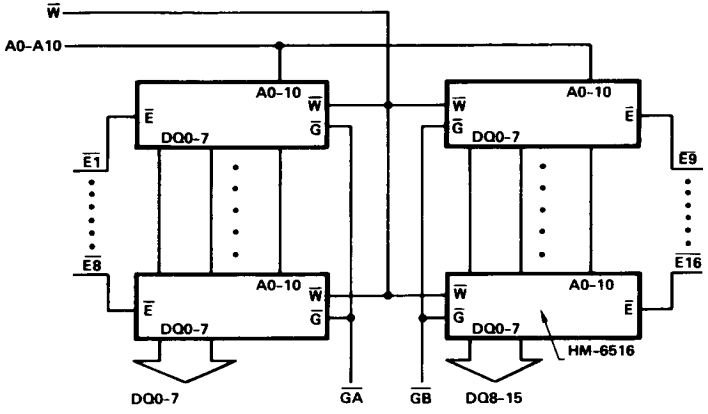
48 LEAD MODULE
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3009**

Functional Diagram



Organizational Guide

FOR 32K x 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K x 16 CONFIGURATION

CONNECT: PIN 6 ($\overline{E1}$) to PIN 15 ($\overline{E9}$)
PIN 7 ($\overline{E2}$) to PIN 24 ($\overline{E10}$)
PIN 8 ($\overline{E3}$) to PIN 25 ($\overline{E11}$)
PIN 9 ($\overline{E4}$) to PIN 34 ($\overline{E12}$)
PIN 10 ($\overline{E5}$) to PIN 35 ($\overline{E13}$)
PIN 11 ($\overline{E6}$) to PIN 38 ($\overline{E14}$)
PIN 12 ($\overline{E7}$) to PIN 39 ($\overline{E15}$)
PIN 14 ($\overline{E8}$) to PIN 40 ($\overline{E16}$)
PIN 13 ($\overline{GA}$) to PIN 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode use the chip enables as if there were only eight, $\overline{E1}$ thru $\overline{E8}$. In the 32K x 8 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. As the HM-92560 is a synchronous memory every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92560 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND-0.3V to VCC+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
Gate Count . . . . . 415250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C

DC Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C (HM-92560-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	(NOTE 1) TEST CONDITIONS
ICCSB	Standby Supply Current	-	500	µA	IO = 0mA, VI = VCC or GND
ICCOP	Operating Supply Current (16K x 16) (Note 2)	-	30	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = VCC or GND, $\overline{G}$ = VCC
ICCOP	Operating Supply Current (32K x 8) (Note 2)	-	15	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = VCC or GND, $\overline{G}$ = VCC
ICCDR	Data Retention Supply Current	-	350	µA	VCC = 2.0V, IO = 0mA, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-5.0	+5.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 3)	VCC-0.4	-	V	IO = -100µA

Capacitance T_A = +25°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CIA	Address Input Capacitance (Note 3)	-	200	pF	f = 1MHz, All measurements are referenced to device GND
CIE1	Enable Input Capacitance (16K x 16) (Note 3)	-	100	pF	
CIE2	Enable Input Capacitance (32K x 8) (Note 3)	-	50	pF	
CIG1	Output Enable Input Capacitance (16K x 16) (Note 3)	-	150	pF	
CIG2	Output Enable Input Capacitance (32K x 8) (Note 3)	-	100	pF	
CIO1	Input/Output Capacitance (16K x 16) (Note 3)	-	150	pF	
CIO2	Input/Output Capacitance (32K x 8) (Note 3)	-	250	pF	
CIW	Write Input Capacitance (Note 3)	-	200	pF	
CCVCC	Decoupling Capacitance	0.5	-	µF	

NOTES:

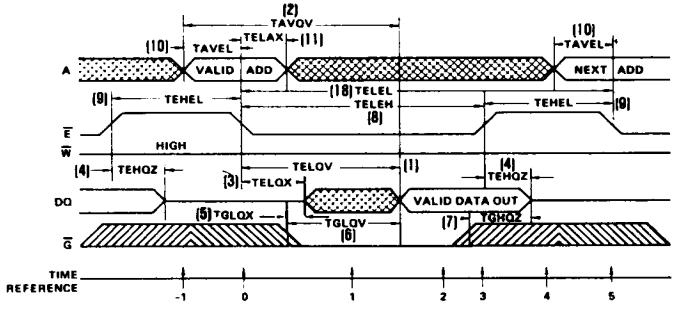
1. VCC = 4.5V and 5.5V
2. Typical derating 5mA/MHz increase in ICCOP.
3. Tested at initial design and after major design changes.

AC Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C (HM-92560-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	150	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	170	ns	(Notes 1, 3)
(3) TELQX	Chip Enable Output Enable Time	10	-	ns	(Notes 2, 3)
(4) TEHQZ	Chip Enable Output Disable Time	-	70	ns	(Notes 2, 3)
(5) TGLQX	Output Enable Output Enable Time	10	-	ns	(Notes 2, 3)
(6) TGLQV	Output Enable Output Valid Time	-	70	ns	(Notes 1, 3)
(7) TGHQZ	Output Enable Output Disable Time	-	70	ns	(Notes 2, 3)
(8) TELEH	Chip Enable Pulse Negative Width	150	-	ns	(Notes 1, 3)
(9) TEHEL	Chip Enable Pulse Positive Width	80	-	ns	(Notes 1, 3)
(10) TAVEL	Address Setup Time	20	-	ns	(Notes 1, 3)
(11) TELAX	Address Hold Time	50	-	ns	(Notes 1, 3)
(12) TWLWH	Write Enable Pulse Width	150	-	ns	(Notes 1, 3)
(13) TWLEH	Write Enable Pulse Setup Time	150	-	ns	(Notes 1, 3)
(14) TELWH	Write Enable Pulse Hold Time	150	-	ns	(Notes 1, 3)
(15) TDVWH	Data Setup Time	80	-	ns	(Notes 1, 3)
(16) TWHDX	Data Hold Time	20	-	ns	(Notes 1, 3)
(17) TWLDV	Write Data Delay Time	70	-	ns	(Notes 1, 3)
(18) TELEL	Read or Write Cycle Time	230	-	ns	(Notes 1, 3)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. VCC = 4.5V and 5.5V.

Read Cycle



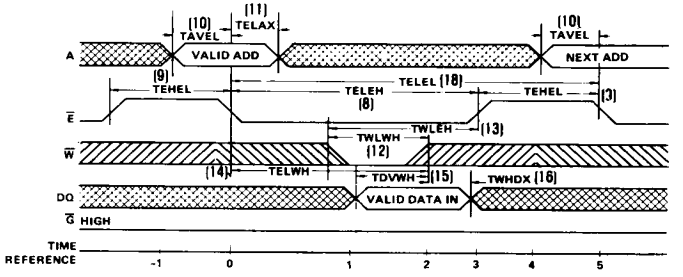
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	X	V	Z	Cycle Begins, Addresses are Latched
1	L	H	L	X	X	Output Enabled
2	L	H	L	X	V	Output Valid
3	↗	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

Read Cycle (Continued)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	
-1	H	X	H	X	X	Memory Disabled
0	↓	X	H	V	X	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Write Period Begins
2	L	↑	H	X	V	Data In is Written
3	↑	H	H	X	X	Write Completed
4	H	X	H	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	H	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TWHDX and TDVWH must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.